What is claimed is:

[Claim 1] A system for critical parameter analysis (CPA) of a semiconductor device (DUT), comprising:

a focused optical beam scanning device for scanning and imaging the semiconductor device (DUT) and for imparting light energy to illuminated portions of the semiconductor device (DUT) during scanning;
automated test apparatus (ATE) for providing predefined stimulus to the semiconductor device (DUT) and for comparing responses from the semiconductor device (DUT) against a set of predefined expected responses; and
a signal generator for providing an output signal indication when the automated test apparatus detects a difference between the responses from the semiconductor device (DUT) and the predefined expected responses,
wherein said focused optical beam scanning device and said ATE are adapted such that both operate upon the semiconductor device simultaneously.

[Claim 2] A system according to claim 1, wherein said semiconductor device (DUT) is fixtured such that ATE connections to the device are made within a scanning chamber of the focused optical beam scanning device.

[Claim 3] A system according to claim 1, wherein said focused optical beam scanning device is a laser scanning microscope (LSM).

[Claim 4] A system according to claim 1, further comprising:

image converting means for representing output from said focused optical beam scanning device as a viewable video signal and for overlaying the output signal indication from the ATE on said viewable video signal; and
display means for viewing said video signal with overlaid ATE output signal indication.

[Claim 5] A system according to claim 4, wherein said overlaid ATE output signal indication produces a visible spot on said display device at a location on a simultaneously displayed image of the semiconductor device (DUT) that indicates the location on the semiconductor device that was illuminated by the optical beam scanning device at the time the ATE output signal indication was produced.

[Claim 6] A system according to claim 1, wherein said predefined stimulus is provided to said automated test apparatus (ATE) in the form of a set of test vectors.

[Claim 7] A system according to claim 1, wherein said predefined responses are provided to said automated test apparatus (ATE) in the form of a set of test vectors.

[Claim 8] A system according to claim 1, wherein said automated test apparatus (ATE) is configured to repeatedly apply said predefined stimulus to said semiconductor device (DUT) in a test "loop".

[Claim 9] A system according to claim 1, wherein said output signal indication is a short pulse generated when a difference is detected between responses by said semiconductor device (DUT) to said predefined stimulus and the predefined expected responses.

[Claim 10] A system according to claim1, wherein said automated test apparatus (ATE) is configured to repeatedly cycle ("short-cycle") said predefined stimulus from a starting point up a point of failure when such failure is detected.

[Claim 11] A method for critical parameter analysis of a semiconductor device, comprising:

providing a focused optical beam scanning device;
disposing a semiconductor device (DUT) within a scanning area of said optical beam scanning device;
providing automated test apparatus (ATE);
connecting said semiconductor device (DUT) to said automated test apparatus (ATE);
providing said automated test apparatus (ATE) with a set of predefined stimuli to be applied to said semiconductor device (DUT);
providing said automated test apparatus (ATE) with a set of predefined expected response from said semiconductor device (DUT);
adapting said automated test apparatus (ATE) to generate an output signal indication of a difference between responses to said predefined stimuli by the semiconductor device (DUT) and the predefined expected responses;
operating said automated test apparatus (ATE) to apply said predefined stimuli to said semiconductor device (DUT) via said connections thereto and to compare responses therefrom against the predefined stimuli; and
operating said optical beam scanning device to image said semiconductor device (DUT) and to apply light energy to imaged portions of said semiconductor device (DUT) via a scanning beam of said optical beam scanning device.

[Claim 12] A method according to claim 11, wherein said semiconductor device (DUT) is fixtured such that ATE connections to the semiconductor device are made within a scanning chamber of the focused optical beam scanning device.

[Claim 13] A method according to claim 12, wherein said focused optical beam scanning device is a laser scanning microscope (LSM).

[Claim 14] A method according to claim 11, further comprising:

displaying on a display device an image representation of said semiconductor device (DUT) produced by said optical beam scanning device; and
overlaying on said image representation a visible indication of said ATE output signal indication.

[Claim 15] A method according to claim 14, wherein said overlaid ATE output signal indication produces a visible spot on said display device at a location on a the displayed image representation of the semiconductor device (DUT) that indicates a location on the semiconductor device that was illuminated by the optical beam scanning device at the time the ATE output signal indication was produced.

[Claim 16] A method according to claim 11, wherein said predefined stimulus and said set of predefined expected response are provided in the form of a set of test vectors.

[Claim 17] A method according to claim 11, further comprising:

configuring said automated test apparatus (ATE) to repeatedly apply said predefined stimulus to said semiconductor device (DUT) in a test "loop".

[Claim 18] A method according to claim 11, further comprising:

configuring said automated test apparatus (ATE) to provide said output signal indication in the form of a short pulse.

[Claim 19] A method according to claim 11, further comprising:

configuring said automated test apparatus (ATE) to repeatedly cycle ("short-cycle") said predefined stimulus from a starting point up a point of failure when such failure is detected.

[Claim 20] A system for critical parameter analysis (CPA) of a semiconductor device (DUT), comprising:

a laser scanning microscope;
automated test apparatus (ATE) for providing predefined stimulus to the semiconductor device (DUT), for comparing responses from the semiconductor device (DUT) against a set of predefined expected responses, and for generating a short output pulse when a difference is detected between responses from said semiconductor device (DUT) and said predefined expected responses;
means for disposing said semiconductor device (DUT) within a scanning chamber of said laser scanning microscope (LSM) while said semiconductor device (DUT) is connected to said automated test apparatus (ATE);
display means for displaying an image of said semiconductor device produced by said laser scanning microscope;
means for overlaying a visible representation of said short output pulse on said displayed image to indicate a corresponding position on the semiconductor device (DUT) of a scanning beam of the laser scanning microscope (LSM) at the time the output pulse was generated; and
means for repeatedly applying said predefined stimulus to said semiconductor device (DUT) and comparing responses therefrom against said predefined expected responses while simultaneously scanning said semiconductor device (DUT) with said laser scanning microscope (LSM).